WHAT IS CLAIMED IS:

1. A method for controlling a memory system using a storage medium, which is inserted into an electronic apparatus via a connector to add a memory function thereto,

said storage medium having ground terminals, power supply terminals, control terminals and data input/output terminals,

said connector having a function of being sequentially connected to each of said terminals,

wherein when said storage medium is inserted into said connector, said ground terminals and control terminals of said storage medium are connected to corresponding terminals of said connector before said power supply terminals and data input/output terminals of said storage medium are connected to corresponding terminals of said connector.

2. A method for controlling a memory system using a storage medium, which is inserted into an electronic apparatus via a connector to add a memory function thereto,

said storage medium having ground terminals, power supply terminals, control terminals and data input/output terminals,

said connector having a function of being sequentially disconnected from each of said terminals,

wherein when said storage medium is ejected from said connector, said power supply terminals and data input/output terminals of said storage medium are disconnected from corresponding terminals of said connector before said ground terminals and control terminals of said storage medium are disconnected from corresponding terminals of said connector.

3. A method for controlling a memory system as set forth in claim 1, wherein a signal transmitted to said control terminal is a command latch enable signal.

ok Cl. 1-9 Taken 6/19/99 435/64 & 924.1

4. A method for controlling a memory system using a storage medium, which is inserted into an electronic apparatus via a connector to add a memory function thereto,

said storage medium having ground terminals, power supply terminals, a first control terminal, a second control terminal and data input/output terminals,

said connector having a function of being sequentially connected to each of said terminals,

wherein when said storage medium is inserted into said connector, said ground terminals and first control terminals of said storage medium are connected to corresponding terminals of said connector before said power supply terminals and data input/output terminal of said storage medium are connected to corresponding terminals of said connector, and

said second control terminal being connected to a corresponding terminal of said connector before said data input/output terminals are connected to a corresponding terminal of said connector.

5. A method for controlling a memory system using a storage medium, which is inserted into an electronic apparatus via a connector to add a memory function thereto,

said storage medium having ground terminals, a power supply terminals, a first control terminal, a second control terminal and data input/output terminals,

said connector having a function of being sequentially connected to each of said terminals,

wherein when said storage medium is ejected from said connector, said data input/output terminals are disconnected from corresponding terminals of said connector before said second control terminal is disconnected from a corresponding terminal of said connector, and

said power supply terminals and data input/output terminals of said storage medium being disconnected from

corresponding terminals of said connector before said ground terminals and first control terminal of said storage medium are disconnected from corresponding terminals of said connector.

6. A method for controlling a memory system having a storage medium, which is inserted into an electronic apparatus via a connector to add a memory function thereto,

said storage medium having ground terminals, power supply terminals, first control terminal, a second control terminal, data input/output terminals and an insertion/ejection detecting terminal,

said connector having a function of being sequentially connected to each of said terminals,

wherein when said storage medium is inserted into said connector, said ground terminals and first control terminals of said storage medium are connected to corresponding terminals of said connector before said power supply terminals and data input/output terminals of said storage medium are connected to corresponding terminals of said connector,

said second control terminal of said storage medium being connected to a corresponding terminal of said connector before said data input/output terminals of said storage medium are connected to corresponding terminals of said connector, and

said insertion/ejection detecting terminal being connected to a corresponding terminal of said connector after all of said terminals of said storage medium are inserted.

7. A method for controlling a memory system having a storage medium, which is inserted into an electronic apparatus via a connector to add a memory function thereto,

said storage medium having ground terminals, power supply terminals, a first control terminal, a second control terminal, data input/output terminals and an

insertion/ejection detecting terminal,

said connector having a function of being sequentially connected to each of said terminals,

wherein when said storage medium is ejected from said connector, said insertion/ejection detecting terminal is disconnected from a corresponding terminal of said connector before said data input/output terminals of said storage medium are disconnected from corresponding terminals of said connector,

said data input/output terminals of said storage medium being disconnected from corresponding terminals of said connector before said power supply terminals and second control terminal of said storage medium are disconnected from corresponding terminals of said connector, and

said power supply terminals of said storage medium being disconnected from corresponding terminals of said connector before said ground terminals and first control terminal of said storage medium are disconnected from corresponding terminals of said connector.

8. A method for controlling a memory system as set forth in claim 7, wherein said storage medium completes the reset of write or erase operation before said power supply terminals of said storage medium are disconnected from the corresponding terminals of said connector after said insertion/ejection detecting terminal of said storage medium is disconnected from the corresponding terminal of said connector.

9. A method for controlling a memory system as set forth in claim 4, wherein a signal transmitted to said first control terminal is a signal for receiving a command, and a signal transmitted to said second control terminal is a signal for inactivating a data output terminal.

10. A method for controlling a memory system which

includes:

logical blocks managed by the system;

physical blocks for storing therein data corresponding to said logical blocks, said physical blocks comprising a plurality of memory cells;

redundant divisions included in a corresponding said physical blocks for storing therein addresses of corresponding said logical blocks; and

physical block areas formed by at least two of said physical blocks,

wherein a logical address/physical address translation table is prepared for managing corresponding relationships between said logical blocks and said physical blocks.

11. A method for controlling a memory system as set forth in claim 10, wherein when a memory access is carried out, said physical blocks corresponding to said logical blocks are selected by referring to said logical address/physical address translation table to read addresses of said physical block areas corresponding to said logical blocks and to read addresses of said corresponding logical blocks stored in said redundant divisions of at least two of said physical blocks forming said physical block area.

12. A method for controlling a memory system as set forth in claim 10, wherein said logical address/physical address translation table is prepared when a power supply is turned on.

13. A method for controlling a memory system, which is a semiconductor memory system for storing a file managed by a first predetermined units, in a storage area divided into second predetermined units,

wherein said semiconductor memory system is controlled so that boundaries between said first predetermined units are arranged on boundaries between

said second predetermined units.

14. A method for controlling a memory system as set forth in claim 13, wherein said second predetermined unit is an erase unit.

15. A method for controlling a memory system which includes:

files managed by the system;

data areas for storing therein the contents of said files; and

management areas for storing therein a corresponding relationships between said files and said data areas,

wherein when said file is erased, it is marked that said data areas corresponding to said management areas are empty area, to erase said corresponding data areas.

16. A method for controlling a memory system which includes:

files managed by the system;

data areas for storing therein the contents of said files; and

management areas for storing therein a corresponding relationships between said files and said data areas,

wherein when said file is erased, it is marked that said data areas corresponding to said management areas are empty area, and the contents of said management areas are detected, on the basis of signals inputted to said memory system, to erase said data areas.

Sub A2 17. A method for controlling a non-volatile semiconductor memory system, which comprises the steps of:

dividing a cell array into a plurality of physical blocks;

storing each information corresponding to relationship between said physical block and logical block which is managed by said system, in each said physical block; and

in order to form a table for managing corresponding relationships between said logical blocks and said physical blocks, in a random access memory in said system, sequentially preparing required corresponding relationships of corresponding relationships between said logical blocks and said physical blocks, in said random access memory in said system in accordance with accesses from a host.

18. A method for controlling a non-volatile semiconductor memory system as set forth in claim 17, wherein said physical blocks are comprised of non-volatile semiconductor memories as flash memories.

19. A method for controlling a non-volatile semiconductor memory system which comprises the steps of:

dividing a cell array of non-volatile semiconductor memory cells into a plurality of physical blocks;

storing each information corresponding to relationship between said physical block and logical block address in each said physical block, which logical blocks are managed by said system,

in order to form an address translation table for managing corresponding relationships between said physical blocks and said logical block addresses, in a random access memory in said memory system,

forming a plurality of areas, each area being formed by an aggregate of at least one of said plurality of physical blocks,

controlling said system so that data in predetermined address of said logical block are stored in said predetermined area,

forming an address translation table corresponding

to said predetermined area in which data in said predetermined address of said logical block are stored, if necessary, when said non-volatile semiconductor memory is accessed.

20. A method for controlling a non-volatile semiconductor memory system which comprises the steps of:

dividing a cell array of non-volatile memory cells into a plurality of physical blocks;

storing each information corresponding to relationship between said physical block and logical block in a storage region of each of said physical blocks, which logical blocks are managed by said system; and

forming a table for managing a corresponding relationship between said logical blocks and said physical blocks of a flash memory, in a random access memory of said memory system,

said method further comprising the steps of:

ensuring an area formed by one or a plurality of physical blocks, on a cell array of said flash memory;

in every memory access time, searching said object area of physical blocks,

forming said table for managing said corresponding relationship between said logical blocks and said physical blocks, on said random access memory of said system,

allowing to select physical blocks corresponding to said logical blocks by using said table.

21. A method for controlling a non-volatile semiconductor memory system, as set forth in claim 20, which further comprises the steps of:

providing a function of selectively replacing a defective physical blocks including defective cells with redundant physical blocks; and

managing said functions, for said each area, so that the number of defective physical blocks is less than or equal

to a predetermined number.

22. A method for controlling a non-volatile semiconductor memory system, which allows any one of various memory units to be detachably mounted in a body of said memory system, said method comprising a step of selecting a corresponding one of various error correcting means of said body in accordance with said one of various memory units mounted in said body, to carry out error correction.

CJCJ 7/9/2000

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